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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/696,410	10/25/2000	Dion Calvin Michael Horvat	99513	4241

28970 7590 03/26/2004

SHAW PITTMAN
IP GROUP
1650 TYSONS BOULEVARD
SUITE 1300
MCLEAN, VA 22102

EXAMINER	
ZHENG, EVA Y	
ART UNIT	**PAPER NUMBER**
2634	9

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/696,410	Applicant(s) HORVAT ET AL.	
	Examiner Eva Yi Zheng	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/25/00*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8,10-11,13,15,17-20,22* is/are rejected.

7)☒ Claim(s) *2,7,9,12,14,16 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. Applicant is required to enter the correct filing date for claiming foreign priority in the Declaration or Oath. According to application number 2,292,463, the correct filing date should be Dec 17, 1999 instead of Dec 17,2000.

Specification

2. The abstract of the disclosure is objected to because on line 2-3, sentence: "The signal if undersampled and quadrature demodulated." is awkward and unclear. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Freeburg et al. (5,950,118).

a) As shown in Fig. 2, regarding claim 1, Freeburg et al. disclose a method for demodulating a frequency-modulated signal, which method comprises the following steps:

- generating a first signal by fixing the modulated signal amplitude at a predetermined level (202);
- generating a second signal by delaying (204) the first signal;
- generating an output signal (116) by determining the cross product of the fixed amplitude signal and the second signal (206);

whereby the output signal is representative of the demodulated signal (abstract).

b) Regarding claim 3, Freeburg et al. disclose the step of fixing the signal amplitude is performed by applying the signal to a limiting amplifier (202 in Fig 2; Col 3, L5-13).

c) Regarding claim 4, Freeburg et al. disclose the step of generating the first signal comprises the following substeps:

• applying the signal to a limiting amplifier (202 in Fig 2);

• digitizing the output of the limiting amplifier (212 in Fig 2);

whereby subsequent steps are performed in the digital signal domain.

5. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Taura et al. (US 6,664,849).

Regarding claim 17, Taura et al. disclose an apparatus for demodulating a frequency modulated signal, the apparatus comprising at least:

- a limiting amplifier (block 6 in Fig. 3), which amplifier's input receives the frequency modulated signal;

- an analog-to-digital converter (block 8 in Fig.3), which converter operationally receives the limiting amplifier output signal and generates a digitized frequency modulated signal;
- a cross-product multiplier (block 27 in Fig. 7) which receives the digitized frequency modulated signal and outputs the cross-product of the digitized frequency to modulated signal with a delayed copy (block 101 in Fig. 7) of the digitized frequency modulated signal to generate a demodulated output signal (output from block 18 in Fig. 7).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freeburg et al. in view of Hattori (5,825,756).

Regarding claim 5, Freeburg et al. disclose all the subject matter as described above except for the specific teaching of a 1-bit adc.

Hattori, on the other hand, disclose a flip-flop acts as a 1-bit analog-to-digital converter (Fig.8).

A 1-bit ADC, also called Delta-Sigma, is a well-known and advanced ADC technologies. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute A/D in the radio receiver by Freeburg

et al. with the one-bit AD converted circuit by Hattori for better and more accurate signal conversions.

8. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freeburg et al. in view of Abbey (US 6,396,953).

a) Regarding claim 6, Freeburg et al. disclose all the subject matter as described above except for the specific teaching of a data slicer.

On the other hand, Abbey discloses the demodulated output signal by applying the output signal to a data slicer (block 16 in Fig 1).

A data pattern recognizer or correlator provides an optimized synchronization signal (abstract, Abbey).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the radio receiver by Freeburg et al. with the data slicer by Abbey for better data/pattern detection and synchronization on the demodulated signals.

b) Regarding claim 8, Abbey discloses the step of applying the data slicer output to a matched filter to reduce the likelihood of errors in the demodulated signal (block 16 in Fig 1).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kammeyer (4,506,228; IDS). in view of Taura et al.

Regarding claim 10, Kammeyer disclose (as shown in Fig. 1)

- digitizing the limited signal using an analog-to-digital converter (55);
- applying the digitized limited signal to a quadrature demodulator to create a first I signal and a first Q signal (as shown in Fig. 1);

- creating a second I signal by delaying the first I signal (61);
- creating a second Q signal by delaying the first Q signal (60);
- generating a first product by multiplying the first I signal by the second Q signal (62);
- generating a second product by multiplying the first Q signal the second I signal (63);
- subtracting the second product from the first product to generate the demodulated signal (64).

Kammeyer disclose all the subject matter as described above except for the specific teaching of a limiting amplifier.

Taura et al. in the same field of endeavor, discloses amplifying the modulated signal using a limiting amplifier (block 6 Fig 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the FM detector by Kammeyer with the limiter amplifier by Taura et al in order to have constant amplitude of IF signal, converted to digital signal, and then demodulated with better quality.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kammeyer (4,506,228). in view of Taura et al. as applied to claim 10 above, and further in view of Hattori.

Regarding claim 11, Kammeyer and Taura et al. disclose all the subject matter as described above except for the specific teaching of a 1-bit adc.

Hattori, on the other hand, disclose a flip-flop acts as a 1-bit analog-to-digital converter (Fig.8).

A 1-bit ADC, also called Delta-Sigma, is a well-known and advanced ADC technologies. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the A/D in FM detector by Kammeyer with the one-bit AD converted circuit by Hattori for better and more accurate signal conversions.

11. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kammeyer (4,506,228). in view of Taura et al. as applied to claim 10 above, and further in view of Abbey.

a) Regarding claim 13, Kammeyer and Taura et al. disclose all the subject matter as described above except for the specific teaching of a data slicer.

On the other hand, Abbey discloses the demodulated output signal by applying the output signal to a data slicer (block 16 in Fig 1).

A data pattern recognizer or correlator provides an optimized synchronization signal (abstract, Abbey).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the FM detector by Kammeyer with the limiter amplifier by Taura et al, and in addition with the data slicer by Abbey for better data/pattern detection and synchronization on the demodulated signals.

b) Regarding claim 15, Abbey discloses the step of applying the data slicer output to a matched filter to reduce the likelihood of errors in the demodulated signal (block 16 in Fig 1).

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taura et al. in view of Hattori.

Regarding claim 18, Taura et al. disclose all the subject matter as described above except for the specific teaching of a 1-bit adc.

Hattori, on the other hand, disclose a flip-flop acts as a 1-bit analog-to-digital converter (Fig.8).

A 1-bit ADC, also called Delta-Sigma, is a well-known and advanced ADC technologies. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the A/D in FM demodulatot by Taura et al. with the one-bit AD converted circuit by Hattori for better and more accurate signal conversions.

13. Claims 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taura et al. in view of Abbey.

a) Regarding claim 20, Taura et al. disclose all the subject matter as described above except for the specific teaching of a data slicer.

On the other hand, Abbey discloses a data slicer with input operably connected to the cross-product multiplier output (block 16 in Fig 1).

A data pattern recognizer or correlator provides an optimized synchronization signal (abstract, Abbey).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the FM modulator by Taura et al. with the data slicer by Abbey for better data/pattern detection and synchronization on the demodulated signals.

b) Regarding claim 22, Abbey discloses a matched filter with input operably connected to the data slicer output, which matched filter provides for correction of errors in the data slicer output (block 16 in Fig 1).

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taura et al. in view of Kammeyer (4,506,228).

Regarding claim 19, Taura et al. disclose all the subject matter as described above except for the specific teaching of a cross-product multiplier. Kammeyer, in the same field of endeavor, discloses the cross-product multiplier is comprised of: (as shown in Fig. 1)

- a quadrature demodulator with an input connected to the analog-to-digital converter (55) output, which quadrature demodulator generates a baseband I output and a baseband Q output;
- a first delay element (61), which element receives the I output of the quadrature demodulator;
- a second delay element (60), which element receives the Q output of the quadrature demodulator;
- a first multiplier (62), which multiplier has as its inputs the I output of the to quadrature demodulator and the output of the second delay element;
- a second multiplier (63), which multiplier has as its inputs the Q output of the quadrature demodulator and the output of the first delay element;
- an inverter which receives the output of the second multiplier (64; subtractor is inherent and function as an inverter in this case) ;

- an adder (64), which adder has as its inputs the output of the first multiplier and Is the output of the inverter;

whereby the adder output is the demodulated signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the FM detector by Kammeyer in the FM demodulator by Taura et al. for capability of construction with known digital electronic components without temperature or aging effects, avoiding calibration or balancing problems, and better quality of the demodulated signals.

Allowable Subject Matter

15. Claims 2, 7, 9, 12, 14, 16 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Yi Zheng whose telephone number is 703-305-8699. The examiner can normally be reached on 7:30-4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-879-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Eva Yi Zheng
Examiner
Art Unit 2634

March 2, 2004

SHUWANG LIU
PRIMARY EXAMINER